			Docket Number (Optional)	Application Number 10/709292					
FAIT	CODM	ATION DISCLOSURE CITATION	BUR920030135US1 Applicant(s)	Not-Yet Assigned					
INE		(Use several sheets if necessary)	Allen et al.						
	•		Filing Date 04/27/04 Concurrently Herewith	Group Art Unit Unknown					
*EXAMINER		OTHER DOCUMENTS (Including Author, Title	le, Date, Pertinent Pages, Etc.)						
INITIAL	<del> </del>	Papadopoulou, E. and Lee, D.T., "Critical area co Circuits and Systems, IEEE Transactions on , Vol.	mputation via Voronoi diagrams," Co	mputer-Aided Design of Integrated					
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\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and

not considered. Include copy of this form with next communication to applicant.

## **ELECTRONIC INFORMATION DISCLOSURE STATEMENT**

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS

**Application Number:** 

Confirmation Number:

First Named Applicant:

Robert Allen

Attorney Docket Number:

BUR920030135US1

Art Unit:

Examiner:

Search string:

( 6178539 or 6247853 or 6317859 ).pn

## **US Patent Documents**

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
NL	1	6178539	2001-01-23	Papadopoulou et al.			
NL	2	6247853	2001-06-19	Papadopoulou et al.			
NL	3	6317859	2001-11-13	Papadopoulou et al.			

## Signature

Examiner Name	Date		
Nelsin Lan	8/29/06		